SYSTEM AND METHOD FOR OPTIMIZING AN INTEGRATED CIRCUIT DESIGN

ABSTRACT

The present invention provides a comprehensive design environment defining a system architecture and methodology that may integrate interconnects, cores, ePLC, re-configurable processors and software into a manageable and predictable system designs that achieve on-time system IC design results meeting desired specifications and budgets. For example, an interscalable interconnect maybe provided that is scalable and isochronous capable. Additionally, an abstract language may be provided to be able to describe interconnecting core functions. Further, a self-programmable chip may be provided that, upon receiving a construct, it could program itself to achieve the desired functionality, such as through the use of on-chip knowledge and the like.